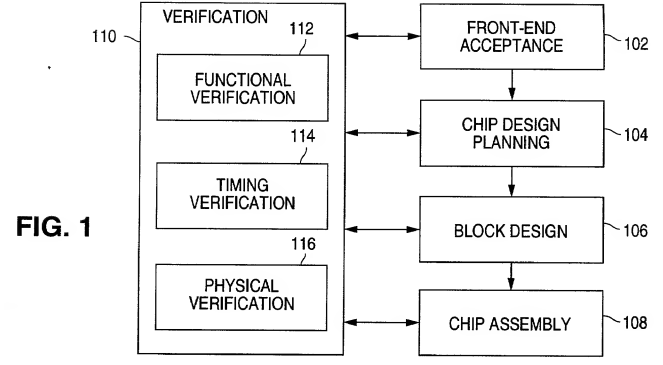


FIG. 1

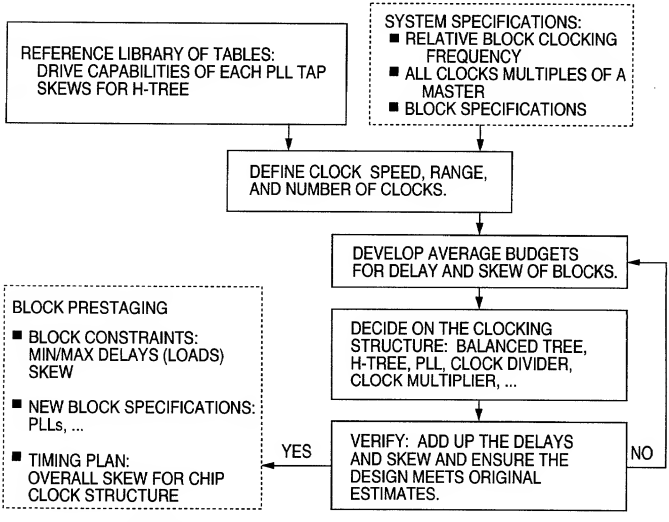


FIG. 3

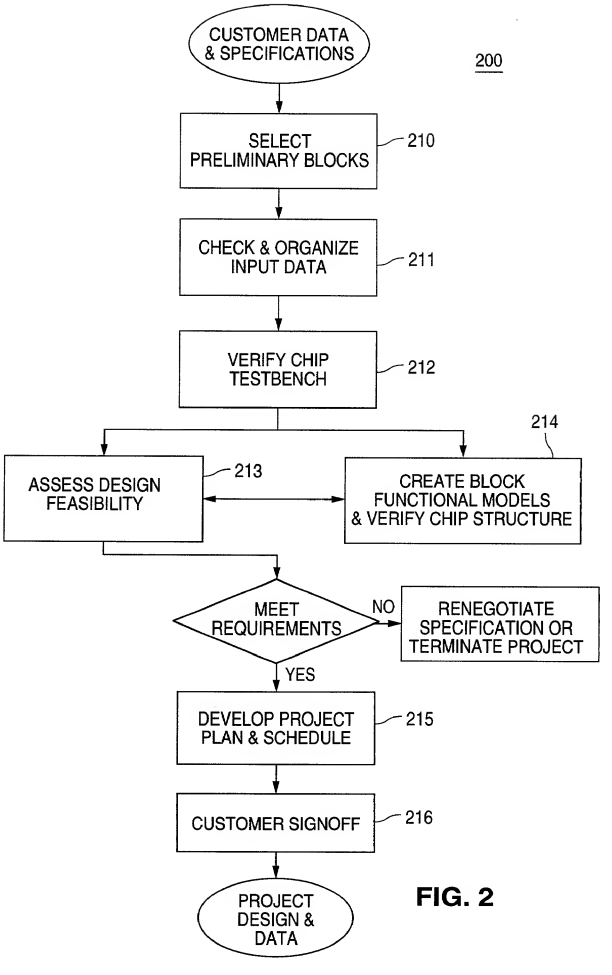


FIG. 2

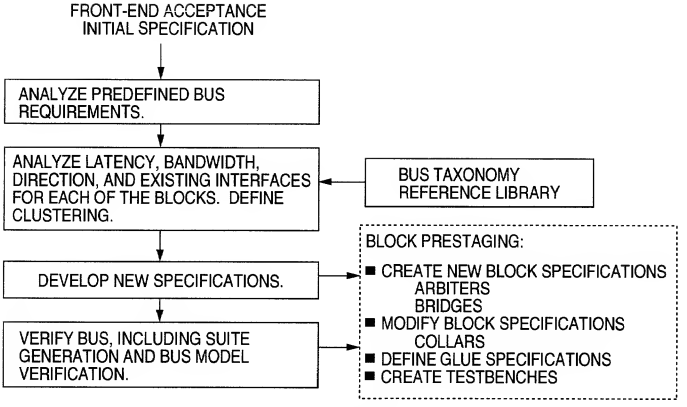


FIG. 4

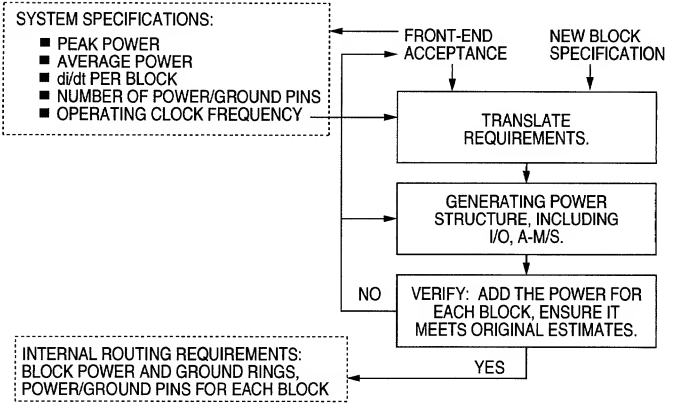


FIG. 5

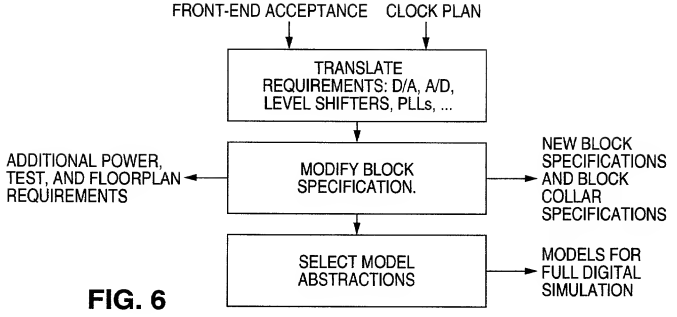


FIG. 6

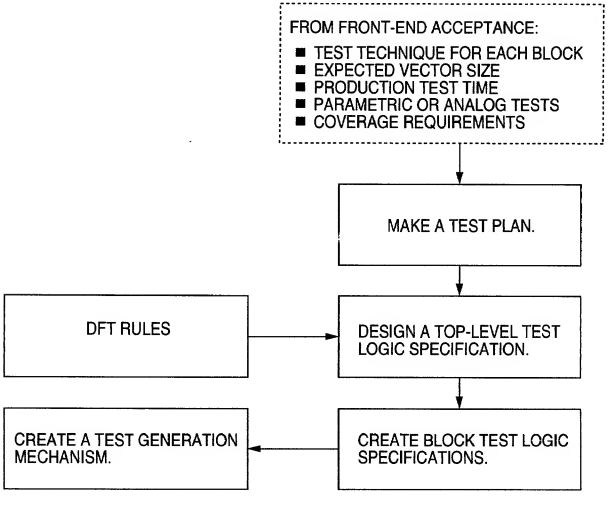


FIG. 7

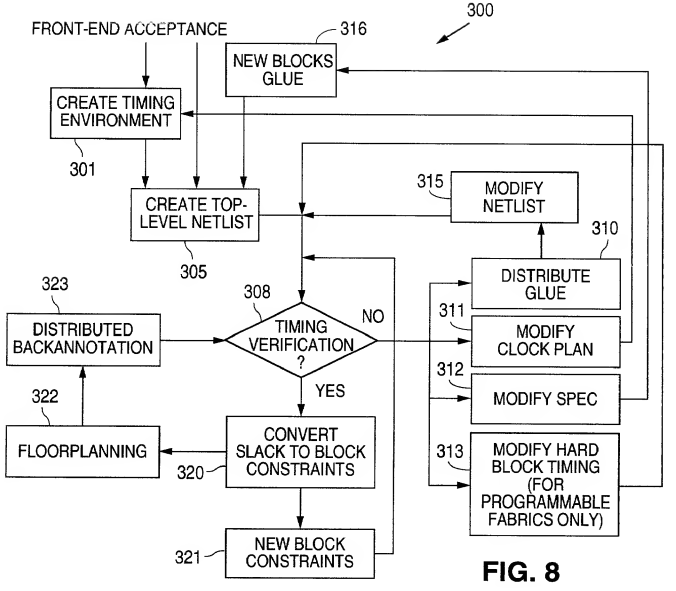


FIG. 8

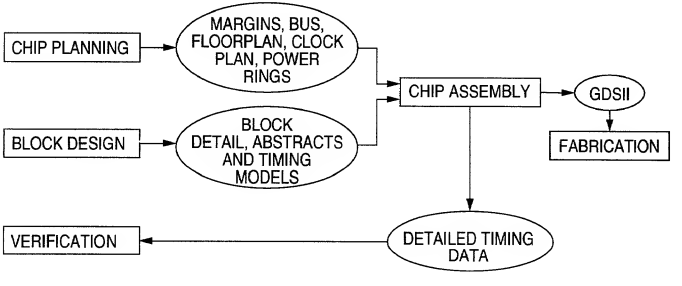


FIG. 10

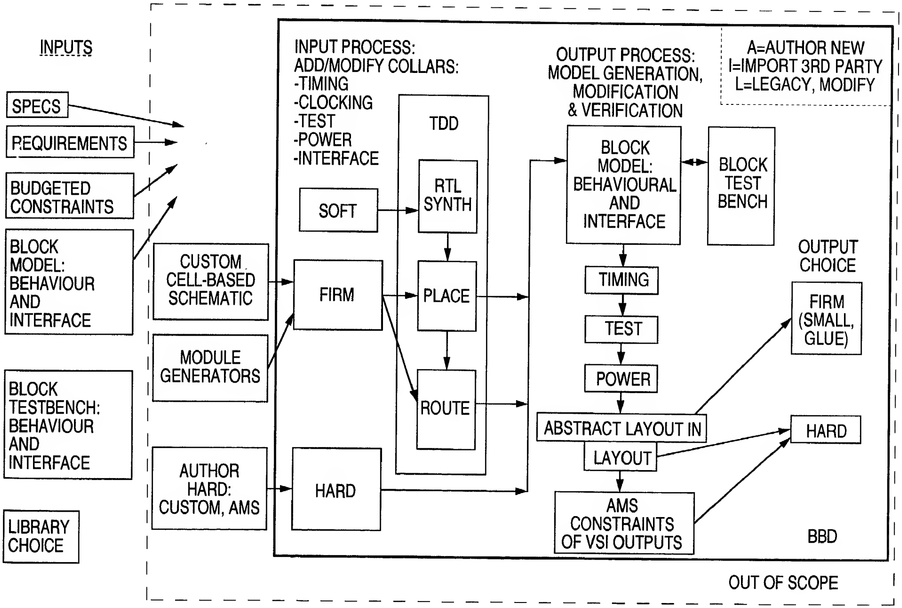

INPUTS
SPECS
REQUIREMENTS
BUDGETED CONSTRAINTS
BLOCK MODEL: BEHAVIOUR AND INTERFACE
BLOCK TESTBENCH: BEHAVIOUR AND INTERFACE
LIBRARY CHOICE
CUSTOM CELL-BASED SCHEMATIC
MODULE GENERATORS
AUTHOR HARD: CUSTOM, AMS
INPUT PROCESS: ADD/MODIFY COLLARS:
-TIMING
-CLOCKING
-TEST
-POWER
-INTERFACE
SOFT
FIRM
HARD
TDD
RTL SYNTH
PLACE
ROUTE
OUTPUT PROCESS: MODEL GENERATION, MODIFICATION & VERIFICATION
BLOCK MODEL: BEHAVIOURAL AND INTERFACE
BLOCK TEST BENCH
TIMING
TEST
POWER
ABSTRACT LAYOUT IN
LAYOUT
AMS CONSTRAINTS OF VSI OUTPUTS
A=AUTHOR NEW
I=IMPORT 3RD PARTY
L=LEGACY, MODIFY
OUTPUT CHOICE
FIRM (SMALL, GLUE)
HARD
BBD
OUT OF SCOPE

FIG. 9

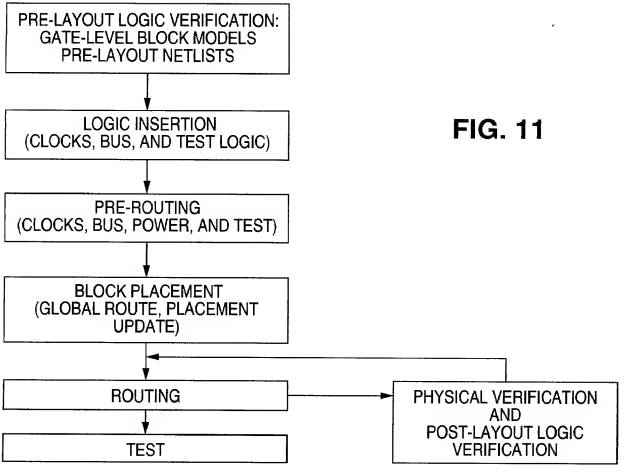


FIG. 11

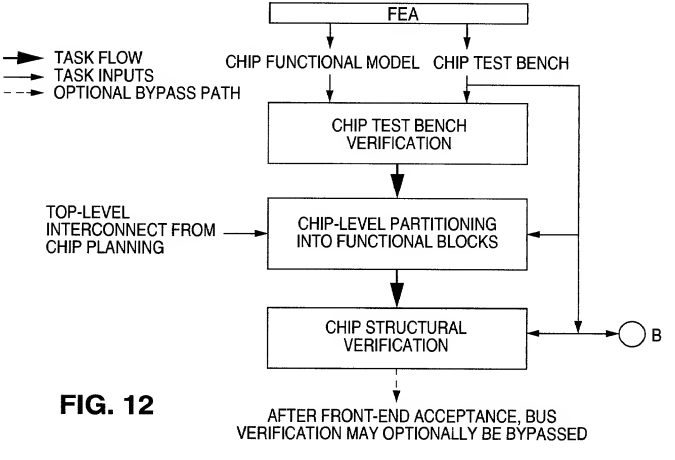


FIG. 12

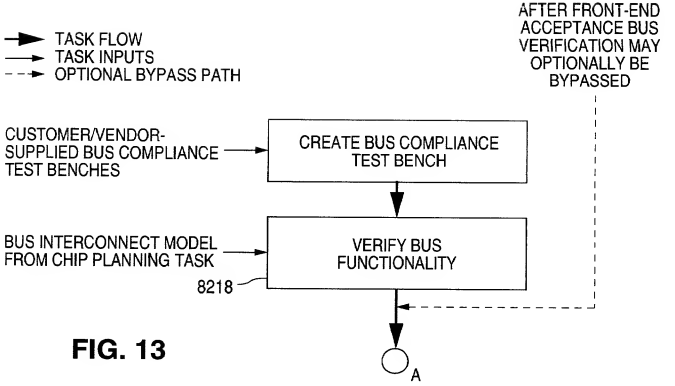

TASK FLOW
TASK INPUTS
OPTIONAL BYPASS PATH
AFTER FRONT-END ACCEPTANCE BUS VERIFICATION MAY OPTIONALLY BE BYPASSED
CUSTOMER/VENDOR-SUPPLIED BUS COMPLIANCE TEST BENCHES
CREATE BUS COMPLIANCE TEST BENCH
BUS INTERCONNECT MODEL FROM CHIP PLANNING TASK
VERIFY BUS FUNCTIONALITY
8218
A

FIG. 13

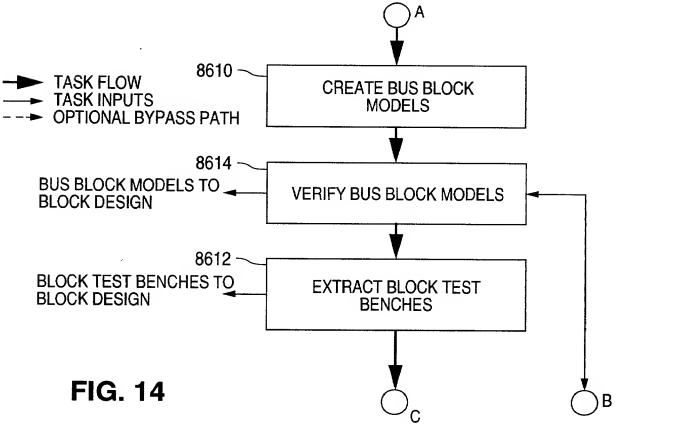

A
TASK FLOW
TASK INPUTS
OPTIONAL BYPASS PATH
8610
CREATE BUS BLOCK MODELS
8614
BUS BLOCK MODELS TO BLOCK DESIGN
VERIFY BUS BLOCK MODELS
8612
BLOCK TEST BENCHES TO BLOCK DESIGN
EXTRACT BLOCK TEST BENCHES
C
B

FIG. 14

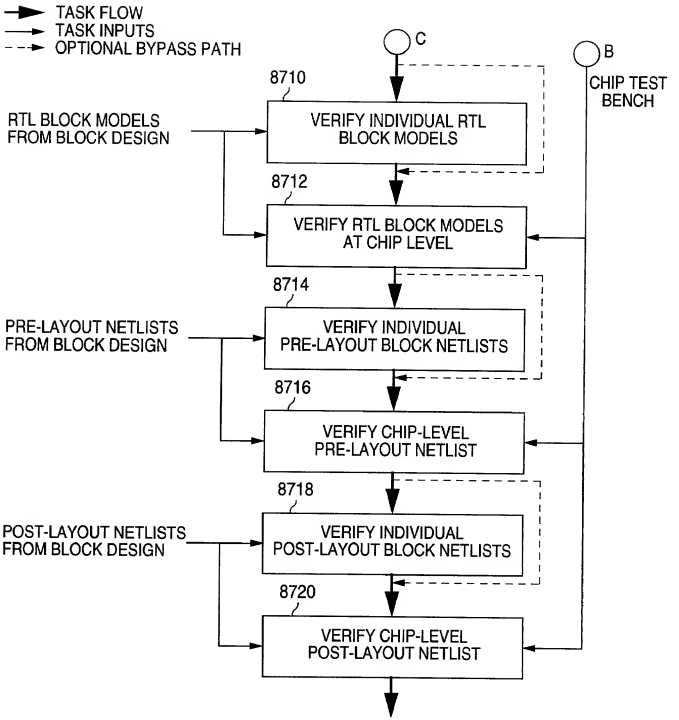

TASK FLOW
TASK INPUTS
OPTIONAL BYPASS PATH
C
B
CHIP TEST BENCH
8710
RTL BLOCK MODELS FROM BLOCK DESIGN
VERIFY INDIVIDUAL RTL BLOCK MODELS
8712
VERIFY RTL BLOCK MODELS AT CHIP LEVEL
8714
PRE-LAYOUT NETLISTS FROM BLOCK DESIGN
VERIFY INDIVIDUAL PRE-LAYOUT BLOCK NETLISTS
8716
VERIFY CHIP-LEVEL PRE-LAYOUT NETLIST
8718
POST-LAYOUT NETLISTS FROM BLOCK DESIGN
VERIFY INDIVIDUAL POST-LAYOUT BLOCK NETLISTS
8720
VERIFY CHIP-LEVEL POST-LAYOUT NETLIST

FIG. 15

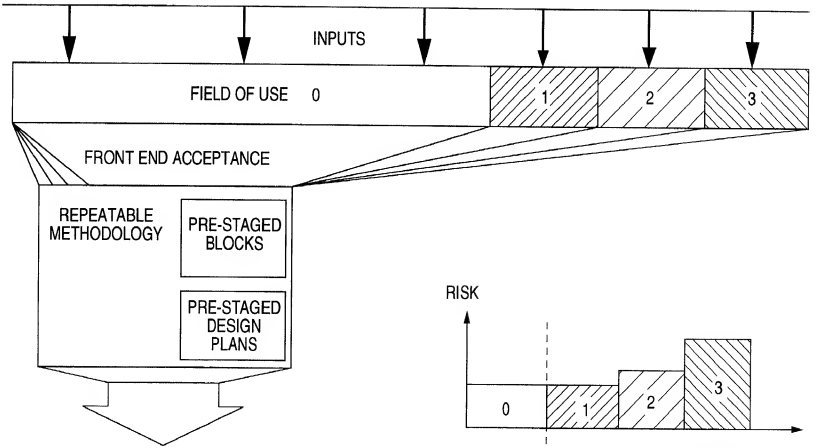


FIG. 16

FIG. 17

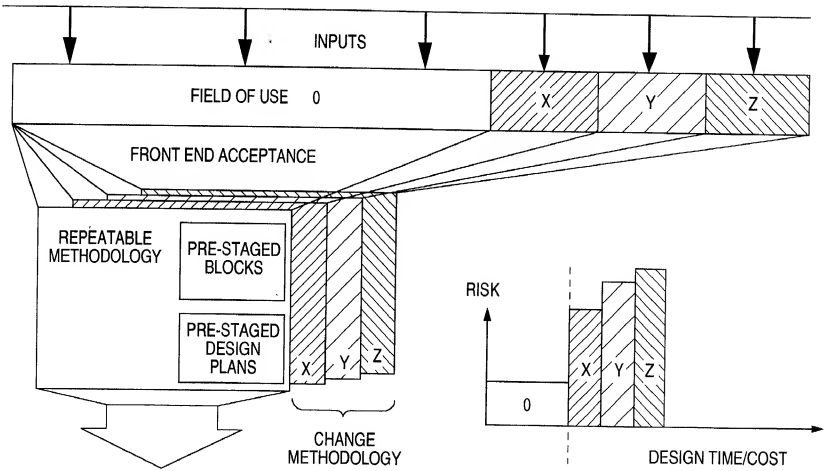


FIG. 18

FIG. 19

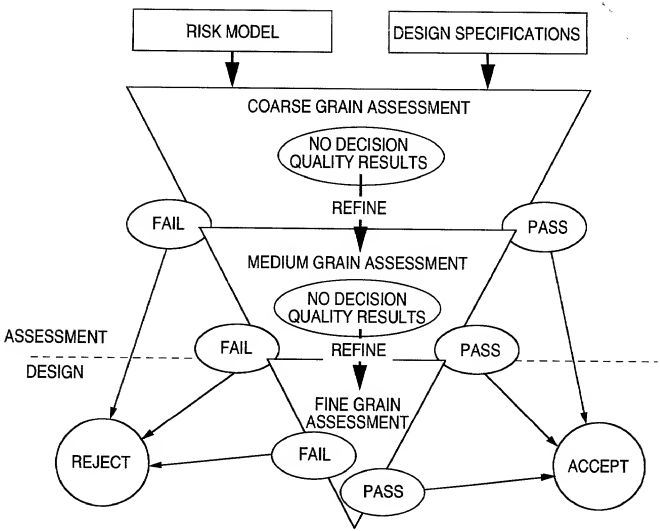


FIG. 20

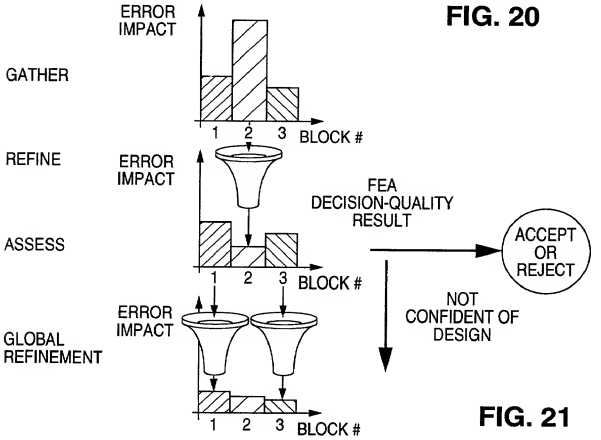


FIG. 21

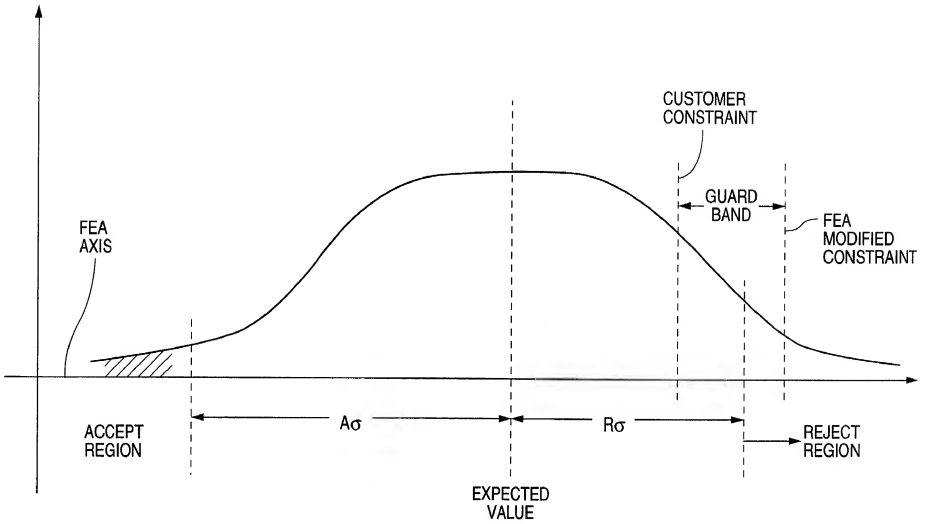


FIG. 22

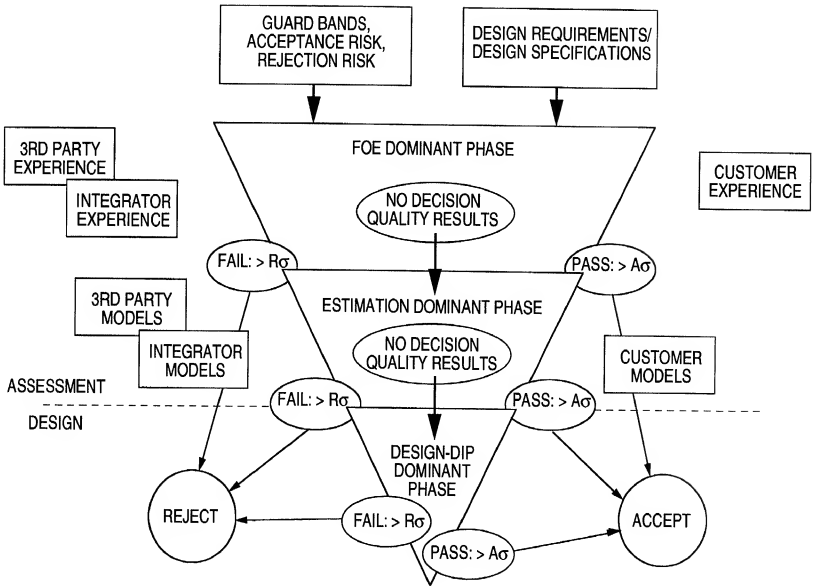


FIG. 23

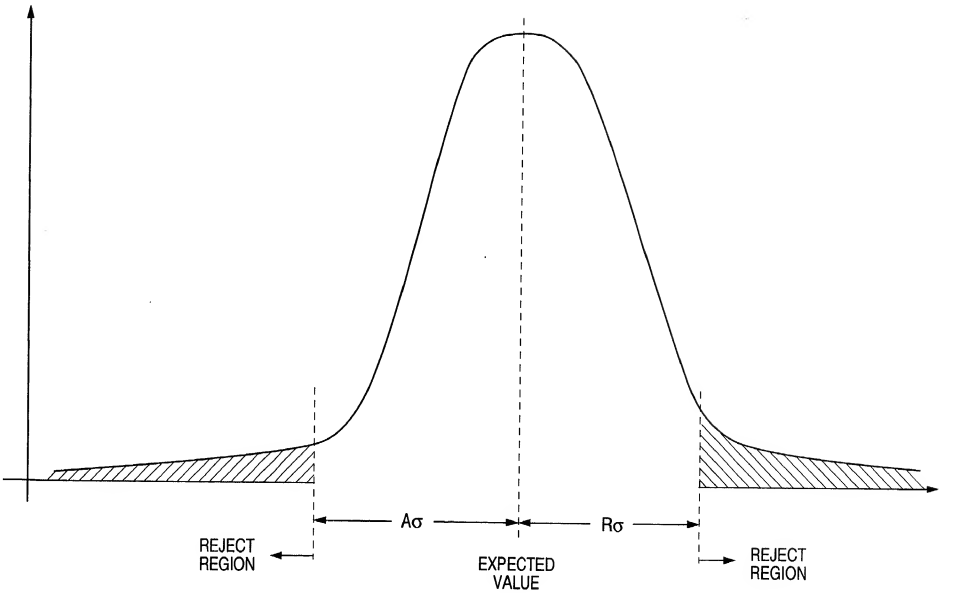


FIG. 24

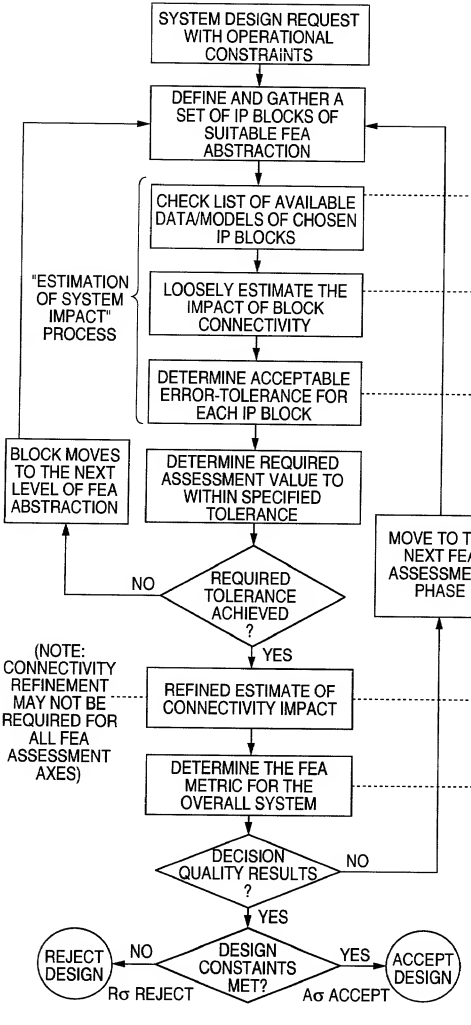


FIG. 25

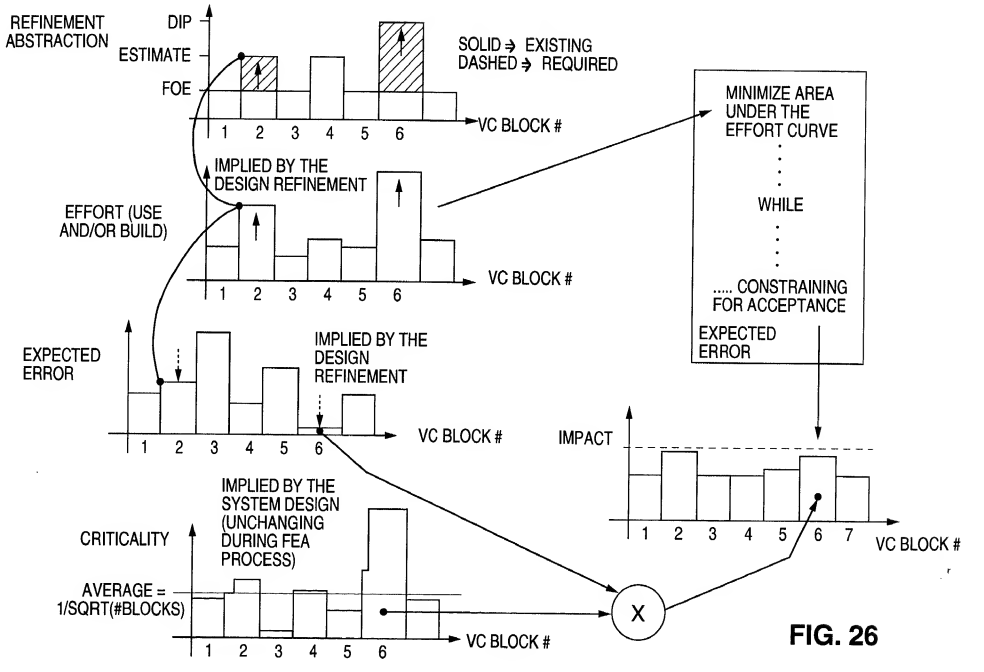

REFINEMENT ABSTRACTION
DIP
ESTIMATE
FOE
SOLID → EXISTING
DASHED → REQUIRED
1 2 3 4 5 6
VC BLOCK #
IMPLIED BY THE DESIGN REFINEMENT
EFFORT (USE AND/OR BUILD)
MINIMIZE AREA UNDER THE EFFORT CURVE
WHILE
..... CONSTRAINING FOR ACCEPTANCE
EXPECTED ERROR
EXPECTED ERROR
IMPLIED BY THE DESIGN REFINEMENT
IMPACT
1 2 3 4 5 6 7
IMPLIED BY THE SYSTEM DESIGN (UNCHANGING DURING FEA PROCESS)
CRITICALITY
AVERAGE = 1/SQRT(#BLOCKS)
X

FIG. 26

ASSESSMENT AXIS	CONSTRAINT TYPE	CONSTRAINT CLASS	ROUTING REFINEMENT	EXAMPLE CRITICALITY MEASURES
POWER	PER MODE OF OPERATION	RELATIVE	MEDIUM	(EXPECTED-BLOCK-POWER ERROR)+ (BLOCK-ROUTING CRITICALITY) * 0.5 * V^2 * E_{BLOCK}
PERFORMANCE	TRANSPORT DELAY	ABSOLUTE	FINE	N/A (I.E., LOCAL-CONNECTION NOT A SYSTEM-SUMMED CRITERIA)
	LATENCY	RELATIVE	MEDIUM	CRITICALITY OF LATENCY-PATH TO SYSTEM: 1/((1-Pr(STARVATION))* ((REQUIRED PATH-LATENCY)- (Σ (BLOCK LATENCY) + Σ (BUS LATENCY)))) CRITICALITY OF BLOCK TO LATENCY PATH: (LATENCY ERROR) / (1-Pr(STARVATION))
	THROUGHPUT	ABSOLUTE	COARSE	N/A (I.E., DOMINATED BY SINGLE BOTTLE-NECK BLOCKS)
AREA	AREA	RELATIVE	MEDIUM	(AREA ERROR) + (BLOCK-ROUTING CRITICALITY)*α
COST	NRE	RELATIVE	COARSE	
	COST PER UNIT	RELATIVE	COARSE	
SCHEDULE	RESOURCE ALLOCATION	MIXED	COARSE	
	DELIVERY TIMELINES	RELATIVE	COARSE	
RISK	POSSIBILITY OF ERROR	MIXED	COARSE	
	IMPACT OF ERROR	MIXED	COARSE	

FIG. 27

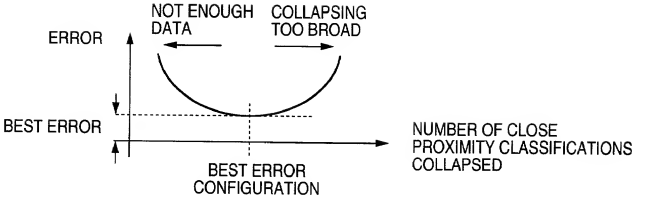


FIG. 28

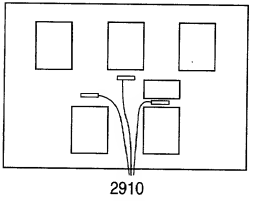


FIG. 29

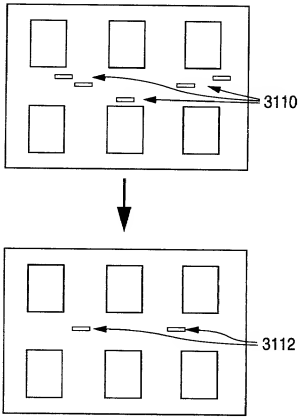


FIG. 31

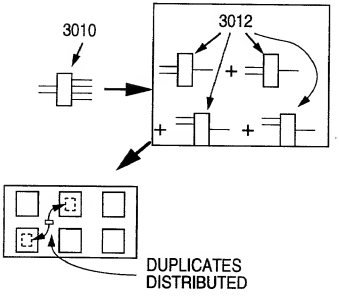


FIG. 30

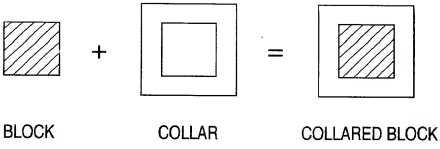


FIG. 32

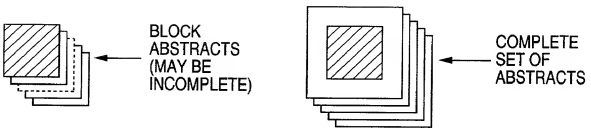


FIG. 33

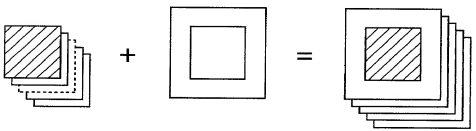
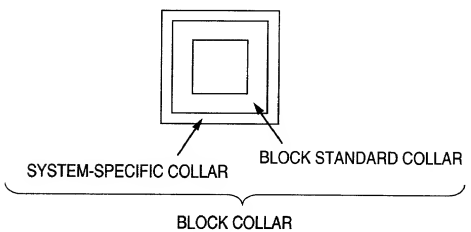


FIG. 34

FIG. 35



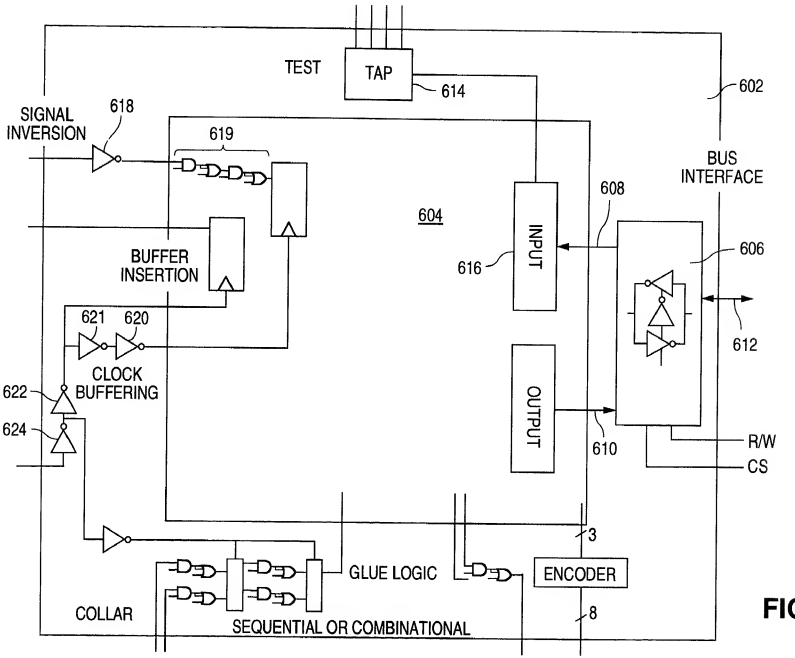


FIG. 36

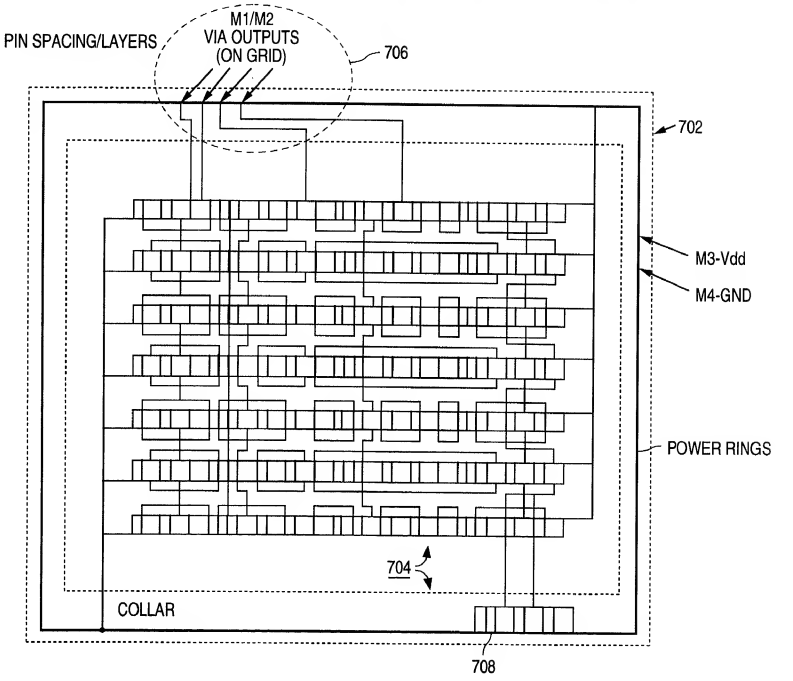

PIN SPACING/LAYERS
M1/M2
VIA OUTPUTS
(ON GRID)
706
702
M3-Vdd
M4-GND
POWER RINGS
704
COLLAR
708

FIG. 37

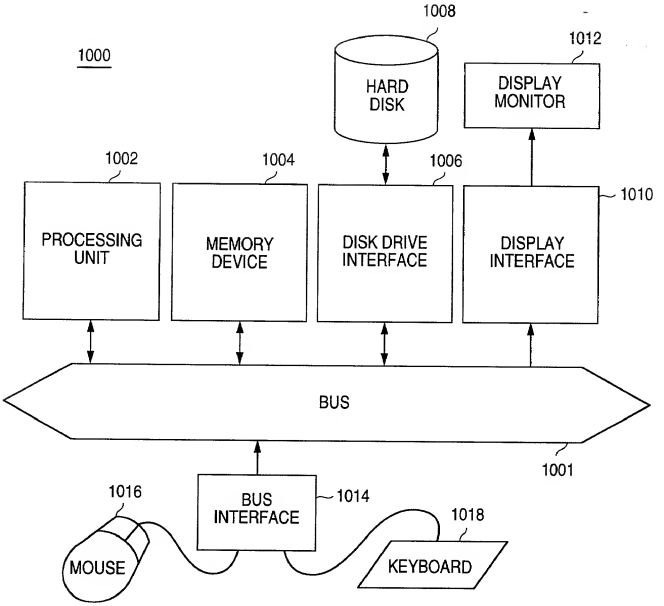


FIG. 38

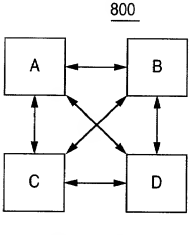


FIG. 39

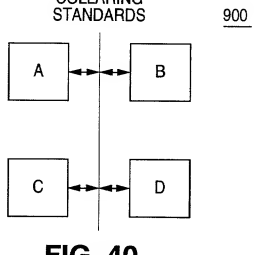


FIG. 40

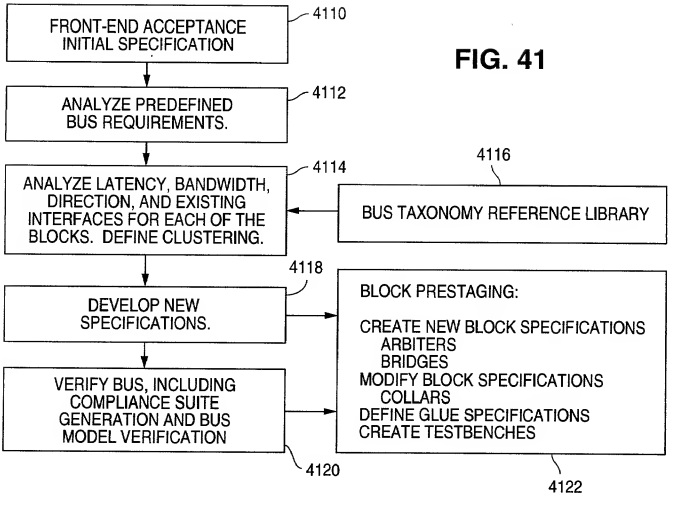


FIG. 41

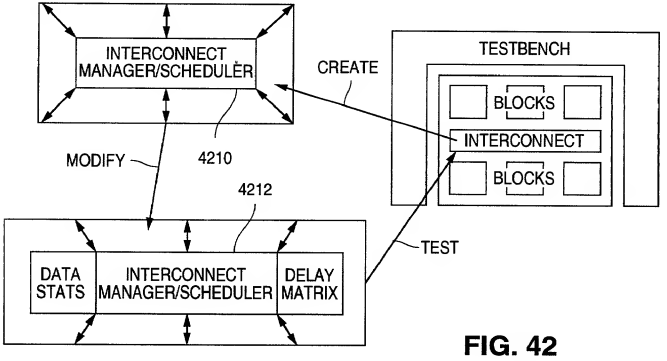


FIG. 42

FROM \ TO	BLOCK 1	BLOCK 2	BLOCK 3	MEMORY	PCI	PIO
BLOCK 1	0	10,000	100	10,000	100	100
BLOCK 2	8,000	0	100	2,000	10,000	100
BLOCK 3	200	100	0	100	200	100
MEMORY	6,000	6,000	100	0	100	100
PCI	6,100	4,100	0	200	0	0
PIO	0	0	0	0	0	0

FIG. 43

FROM \ TO	BLOCK 1	BLOCK 2	BLOCK 3	MEMORY	PCI	PIO
BLOCK 1	0	200	25	200	4	25
BLOCK 2	160	0	100	40	200	25
BLOCK 3	25	100	0	25	25	25
MEMORY	120	180	25	0	6	25
PCI	122	82	0	50	0	0
PIO	0	0	0	0	0	0

FIG. 44

FROM \ TO	BLOCK 1	BLOCK 2	BLOCK 3	MEMORY	PCI	PIO
BLOCK 1	n/a	50	1,000	50	100	1,000
BLOCK 2	50	n/a	1,000	300	100	1,000
BLOCK 3	1,000	1,000	n/a	500	500	1,000
MEMORY	50	50	500	n/a	100	1,000
PCI	100	100	n/a	50	n/a	n/a
PIO	n/a	n/a	n/a	n/a	n/a	n/a

FIG. 45

FROM \ TO	SITE 1	SITE 2	SITE 3	SITE 4	SITE 5	SITE 6
SITE 1	0	1	4	9	16	25
SITE 2	1	0	1	4	9	16
SITE 3	4	1	0	1	4	9
SITE 4	9	4	1	0	1	4
SITE 5	16	9	4	1	0	1
SITE 6	25	16	9	4	1	0

FIG. 46

FROM \ TO	PC1	BLOCK 2	BLOCK 1	MEMORY	BLOCK 3	PIO
PCT	0	4,100	6,100	200	0	0
BLOCK 2	10,000	0	8,000	2,000	100	100
BLOCK 1	100	10,000	0	10,000	100	100
MEMORY	100	6,000	6,000	0	100	100
BLOCK 3	200	100	200	100	0	100
PIO	0	0	0	0	0	0

FIG. 47

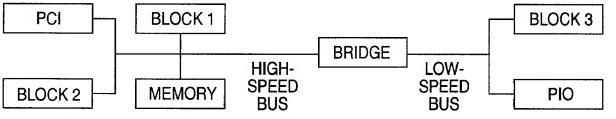


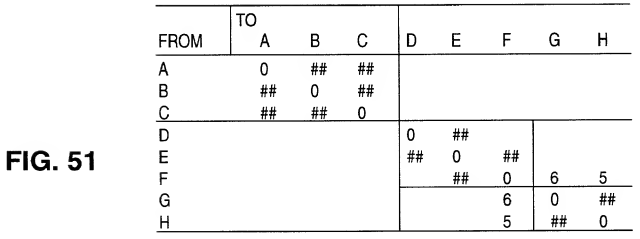
FIG. 48

FIG. 49

FROM \ TO	A	B	C	D	E	F	G	H
A	0	##	##					
B	##	0	##					
C	##	##	0					
D				0	##			
E				##	0	##		
F					##	0	6	5
G						6	0	##
H						5	##	0

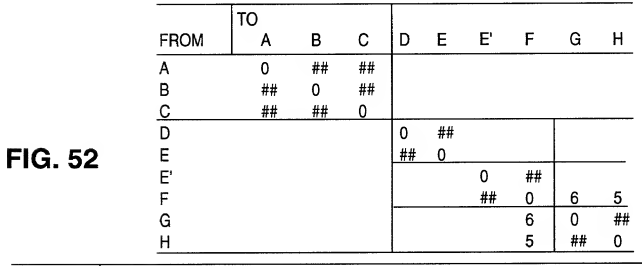
FIG. 50

FROM \ TO	A	B	C	D	E	F	G	H
A	0	##	##					
B	##	0	##					
C	##	##	0					
D				0	##			
E				##	0	##		
F					##	0	6	5
G						6	0	##
H						5	##	0



FROM	TO A	B	C	D	E	F	G	H
A	0	##	##					
B	##	0	##					
C	##	##	0					
D				0	##			
E				##	0	##		
F					##	0	6	5
G						6	0	##
H						5	##	0

FIG. 51



FROM	TO A	B	C	D	E	E'	F	G	H
A	0	##	##						
B	##	0	##						
C	##	##	0						
D				0	##				
E				##	0				
E'						0	##		
F						##	0	6	5
G							6	0	##
H							5	##	0

FIG. 52

FROM	TO PCI	BLOCK 2	BLOCK 1	MEMORY	BLOCK 3	PIO
PCI	0	4,100	6,100	200	0	0
BLOCK 2	10,000	0	8,000	2,000	100	100
BLOCK 1	100	10,000	0	10,000	100	100
MEMORY	100	6,000	6,000	0	100	100
BLOCK 3	200	100	200	100	0	100
PIO	0	0	0	0	0	0

FIG. 53

FROM	TO PCI	BLOCK 2	BLOCK 1	MEMORY	BLOCK 3	PIO
PCI	0	4,100	6,100	200	0	0
BLOCK 2	10,000	0	8,000	2,000	100	100
BLOCK 1	100	10,000	0	10,000	100	100
MEMORY	100	6,000	6,000	0	100	100
BLOCK 3	200	100	200	100	0	100
PIO	0	0	0	0	0	0

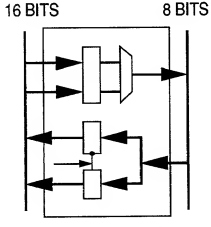
FIG. 54

FROM	TO BUS 1	BUS 2
BUS 1	62,600	600
BUS 2	600	100

FIG. 55

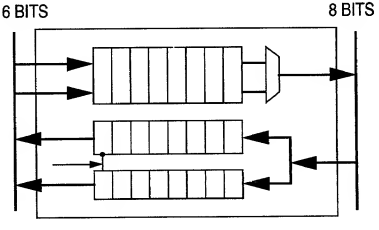
FROM	TO BLOCK 1	BLOCK 2	BLOCK 3	MEMORY	PCI	PIO
BLOCK 1	n/a	31	988	31	91	988
BLOCK 2	31	n/a	997	281	81	988
BLOCK 3	976	997	n/a	488	476	988
MEMORY	31	38	488	n/a	94	988
PCI	81	81	n/a	49	n/a	n/a
PIO	n/a	n/a	n/a	n/a	n/a	n/a

FIG. 56



8 TO 16 BIT BRIDGE

FIG. 57



BRIDGE WITH 8 DEEP FIFOs

FIG. 58

BUS TYPE	UTILIZATION MIN	UTILIZATION MAX	LATENCY DATA	LATENCY TRANSFER
1. SERIAL, ASYNCHRONOUS, CLOCK-REGENERATED BUS	5%	25%	50	200
2. MULTIPLE-LINE ASYNCHRONUS CLOCK-REGENERATED BUS	5%	25%	20	100
3. MULTIPLE-LINE SYNCHRONOUS BUS WITH COMBINED DATA AND ADDRESS LINES	10%	25%	5	25
4. SYNCHRONOUS BUS WITH SEPARATE DATA AND ADDRESS LINES	25%	50%	2.5	10
5. BIDIRECTIONAL BUS WITH SINGLE-LEVEL PIPELINED DATA AND ADDRESS LINES	25%	75%	2	5
6. MULTIPLE-LEVEL PIPELINED BUS WITH SOPHISTICATED ARBITRATION	50%	75%	1.5	2.5
7. CROSSBAR SWITCH	75%	100%	1	2
8. POINT-TO-POINT UNIDIRECTIONAL WIRE	100%	100%	0.5	1

FIG. 59

PARAMETER	NORMAL MODE	TEST MODE	ISOLATION MODE	BOUNDARY MODE
TEST MODEL	BSR MODE=0	BSR MODE=1	BSR MODE=1	BSR MODE=1
TEST CONTROLLER DESIGN	JTAG ir = bypass	JTAG ir=vc_test	JTAG ir=vc_isol	JTAG ir=udl_test
TEST ISOLATION	N/A	OUTPUT ISOLATION	INPUT ISOLATION	INPUT ISOLATION
TEST VALIDATION	FUNCTIONAL TESTBENCH	VC TEST VECTORS	INPUT ISOLATION	UPDATE BYPASS

FIG. 60

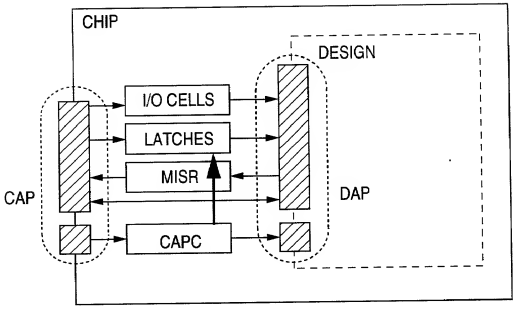


FIG. 61

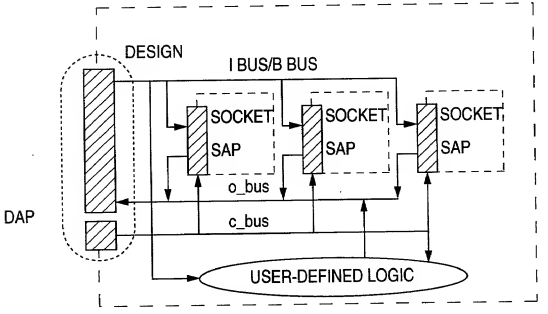


FIG. 62

GENERIC ARCHITECTURE	TARGETED BLOCKS	TEST INTERFACE	TEST METHOD
TEST BUS	LEGACY BLOCKS, NON-SCAN BLOCKS	DIRECT ACCESS FROM CHIP I/O	FUNCTIONAL VECTORS
BSR	SCAN-BASED BLOCKS	MULTIPLE SCAN + BSR CHAINS	CONCATENATED SCAN VECTORS
BIST	REGULAR BLOCKS SUCH AS RAM AND FIFO	BIST CONTROLLER	BUILT-IN ALGORITHMIC TEST PATTERNS
	BUILT-IN LOGIC BIST SUCH AS FULL SCAN	BIST CONTROLLER FOR PRPG/MISR	BUILT-IN RANDOM TEST PATTERNS
TAP	BUILT-IN DEBUG AND DIAGNOSTIC BLOCKS	TAP (TDI, TRST, TMS, TCK, TDO)	JTAG PROTOCOLS

FIG. 63

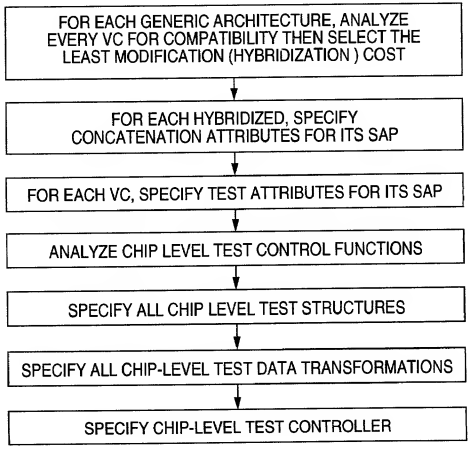


FIG. 64

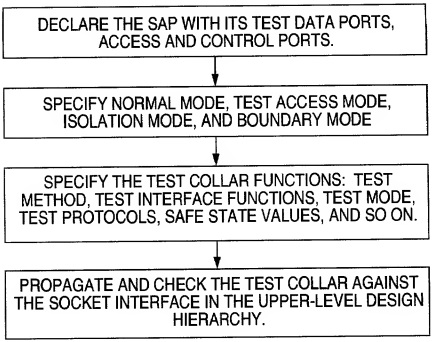


FIG. 65

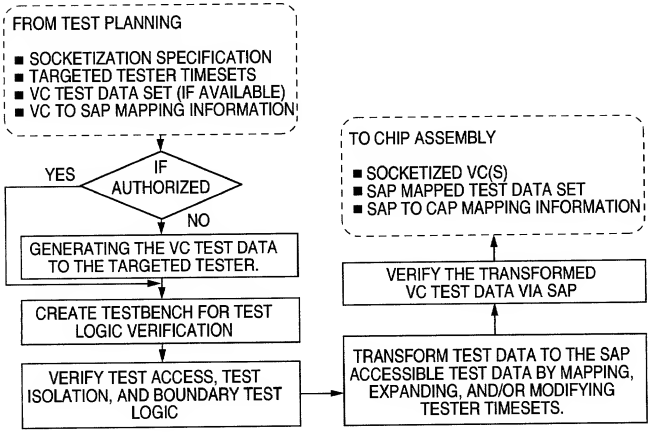


FIG. 68

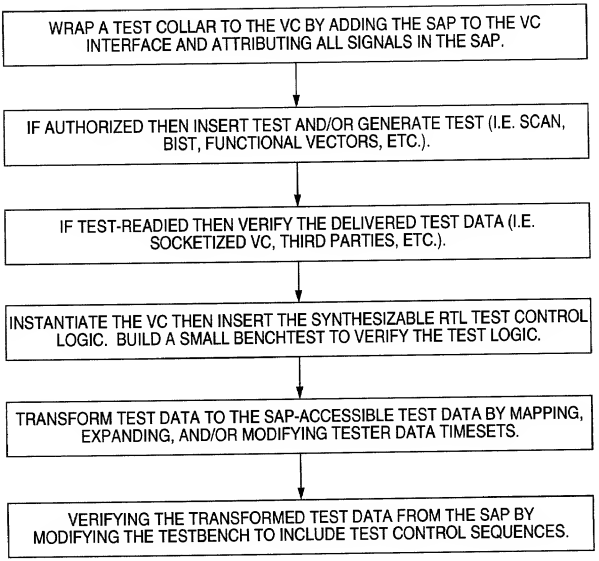


FIG. 66

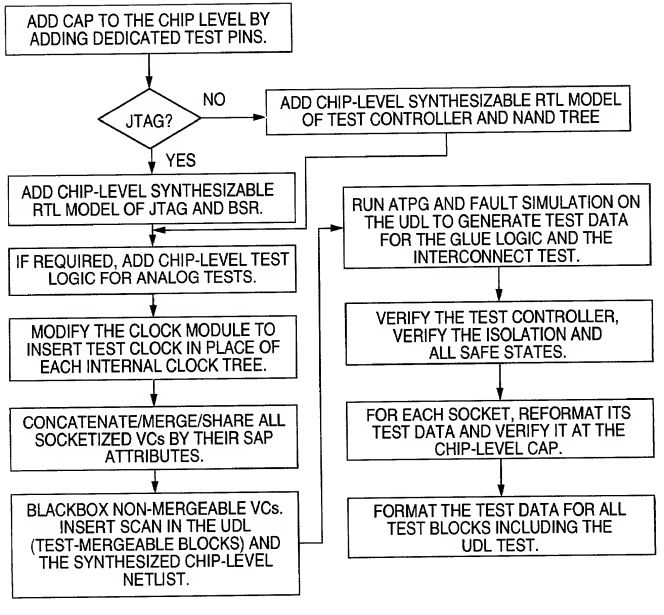


FIG. 67

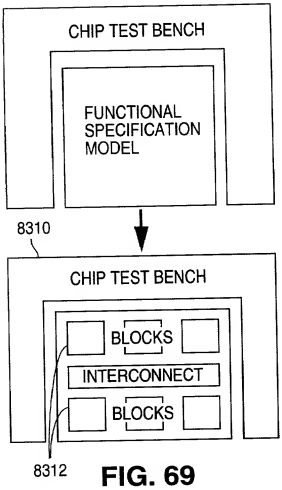


FIG. 69

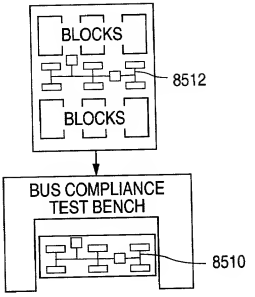


FIG. 70

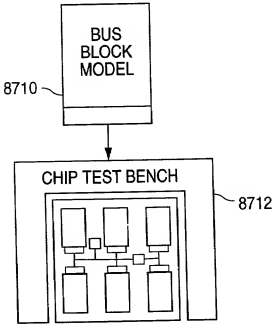


FIG. 71

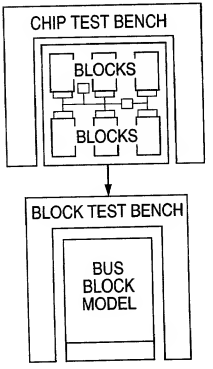


FIG. 72

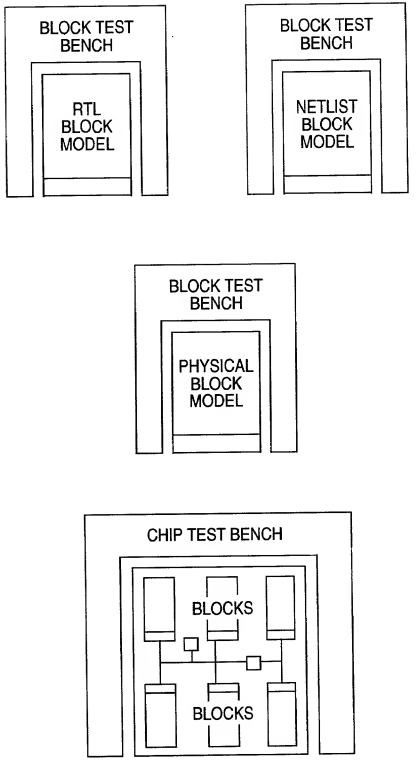


FIG. 73

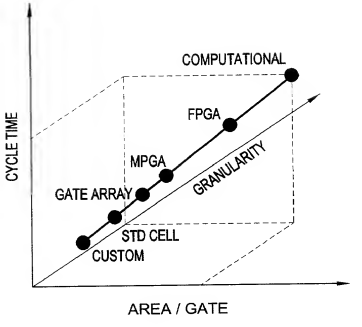


FIG. 74

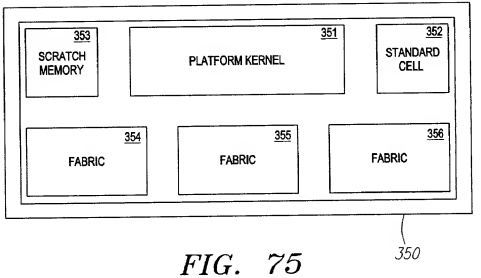


FIG. 75

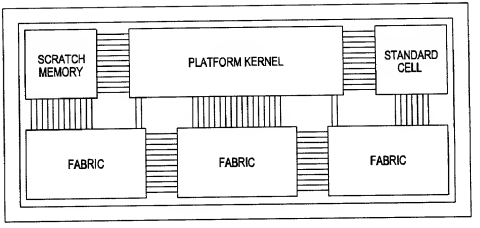


FIG. 76

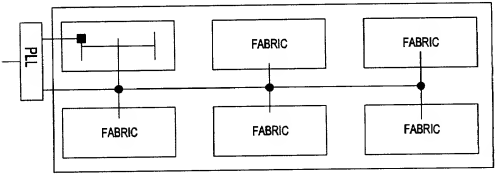


FIG. 77

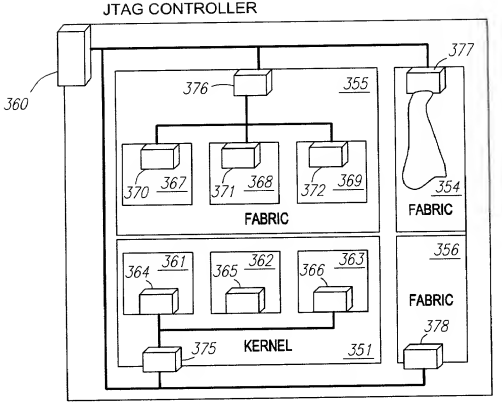


FIG. 78

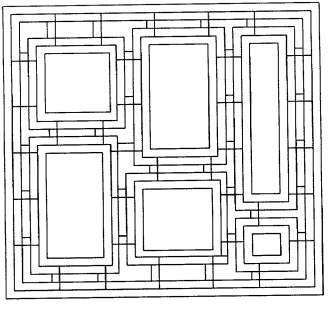


FIG. 79

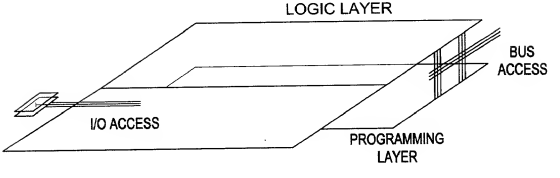
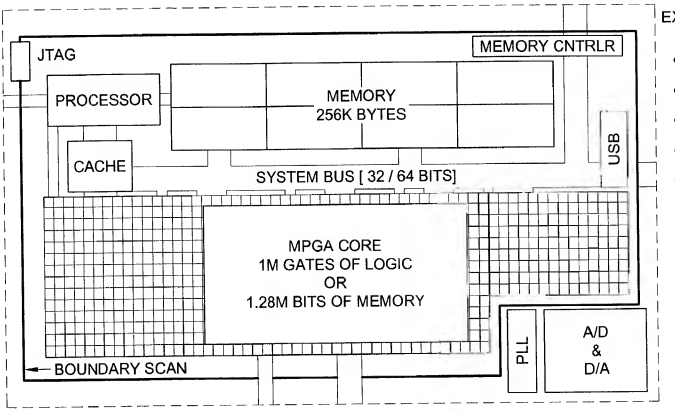


FIG. 80



EXAMPLE PLATFORM:

- 32 BIT PROCESSOR
- A/D & D/A
- 32/64 BIT BUS
- USB & MEM CTLR
- KERNEL MODEL
- MPGA:
- USER CUSTOMIZED
  - SOFTWARE
  - MPGA HARDWARE

FIG. 81

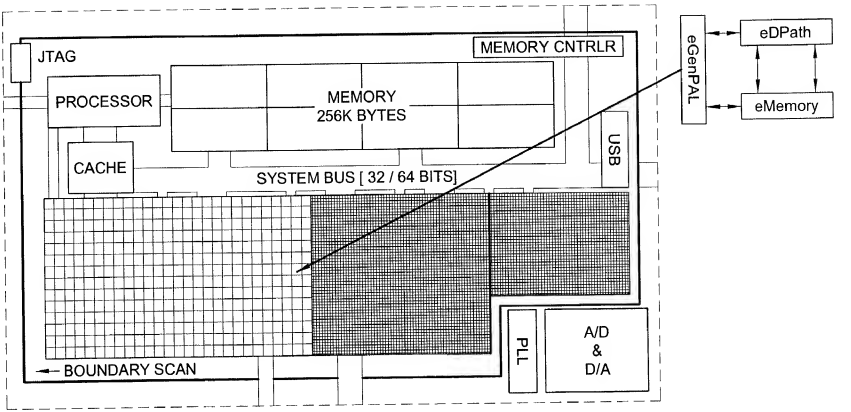
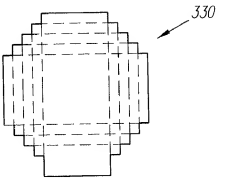


FIG. 82

ATTRIBUTE > / FABRIC v	NRE	FLEXIBILITY	SIZE	POWER	PERFORMANCE	UNIT COST
CUSTOM	HIGH	LOWEST	SMALLEST	LOWEST	HIGHEST	LOWEST
STD. CELL	HIGH	LOW	SMALL	LOW	HIGH	LOW
MPGA	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM
FPGA	LOW	HIGH	LARGE	HIGH	LOW	HIGH
COMPUTATIONAL	LOW	HIGHEST	LARGEST	HIGHEST	LOWEST	HIGHEST

FIG. 83

FIG. 84



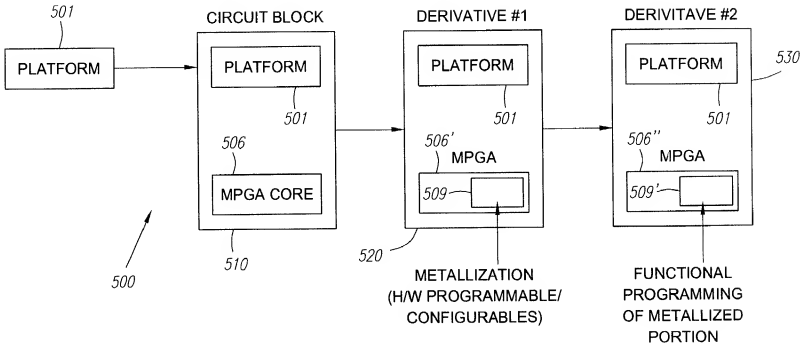
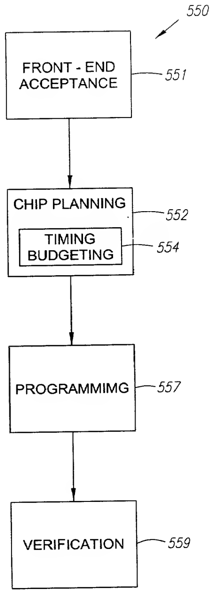
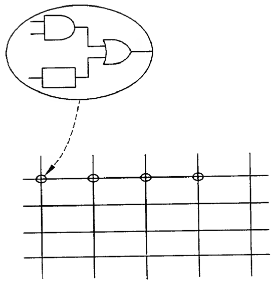

501
PLATFORM
CIRCUIT BLOCK
PLATFORM
501
506
MPGA CORE
510
500
DERIVATIVE #1
PLATFORM
501
506'
MPGA
509
520
METALLIZATION
(H/W PROGRAMMABLE/
CONFIGURABLES)
DERIVITAVE #2
PLATFORM
530
501
506''
MPGA
509'
FUNCTIONAL
PROGRAMMING
OF METALLIZED
PORTION

FIG. 85



DERIVATIVE DESIGN
PROCESS FLOW

FIG. 86



MPGA FABRIC

FIG. 87